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1. An integrated circuit manufactured by the method comprising the acts of:

(a.) providing a partially fabricated integrated circuit structure;

(b.) applying and curing spin-on glass, to form a first dielectric layer;

(c.) depositing dielectric material, to form a second dielectric layer over said first dielectric layer;

(d.) applying and curing spin-on glass, to form a third dielectric layer, to produce a stack including said third dielectric layer over said first and second dielectric layers;

(e.) performing a global etchback to substantially remove portions of said dielectric stack from high points of said partially fabricated structure, wherein at least a portion of said third dielectric layer remains after said global etchback;

(f.) deposition of an interlevel dielectric at least over said remaining third dielectric layer;

(g.) etching holes in said interlevel dielectric in predetermined locations; and

(h.) depositing and patterning a metallization layer to form a desired pattern of connections, including connections through said holes.

2. The integrated circuit of claim 1, wherein said deposition step (c.) is plasma-enhanced.

3. The integrated circuit of claim 1, wherein said deposition step (c.) uses TEOS as a source gas.

4. The integrated circuit of claim 1, comprising the additional step of applying a passivating dielectric, under vacuum conditions, after said step (a.) and Am before said deposition step (b.).

5. The integrated circuit of claim 1, Hi wherein said deposition step (b.) applies said spin-on glass with a thickness in the range of 1000–5000 Å inclusive.

6. The integrated circuit of claim 1, wherein said deposition step (d.) applies said spin-on glass with a thickness in the range of 1000–5000 Å inclusive.

7. The integrated circuit of claim 1, wherein said interlevel dielectric is a doped silicate glass.

8. An integrated circuit manufactured by the method comprising the acts of:

(a.) providing a partially fabricated integrated circuit structure;

(b.) applying and curing spin-on glass, to form a first dielectric layer;

(c.) depositing silicon dioxide, to form a second dielectric layer over said first dielectric layer;

(d.) applying and curing spin-on glass, to form a third dielectric layer to produce a dielectric stack including said third dielectric layer over said first and second layers;

(e.) performing a global etchback to substantially remove said dielectric stack from high points of said partially fabricated structure, wherein at least a portion of said spin-on glass of said third dielectric layer remains after said global etchback;

(f.) deposition of an interlevel dielectric at least over said remaining spin-on glass of said third dielectric layer;

(g.) etching holes in said interlevel dielectric in predetermined locations; and

(h.) depositing and patterning a metallization layer to form a desired pattern of connections, including connections through said holes.

9. The integrated circuit of claim 8, wherein said deposition step (c.) is plasma-enhanced.

10. The integrated circuit of claim 8, wherein said deposition step (c.) uses TEOS as a source gas.

11. The integrated circuit of claim 8, comprising the additional step of applying a passivating dielectric, under vacuum conditions, after said step (a.) and before said deposition step (b.).

12. The integrated circuit of claim 8, wherein said deposition step (b.) applies said spin-on glass with a thickness in the range of 1000–5000 Å inclusive.

13. The integrated circuit of claim 8, wherein said deposition step (d.) applies said spin-on glass with a thickness in the range of 1000–5000 Å inclusive.

14. The integrated circuit of claim 8, wherein said interlevel dielectric is a doped silicate glass.

15. An integrated circuit manufactured by the method comprising the acts of:

(a.) providing a partially fabricated integrated circuit structure;

(b.) applying and curing spin-on glass, to form a first dielectric layer;

(c.) depositing dielectric material, to form a second dielectric layer over said first dielectric layer, said second dielectric layer having a thickness equal to or less than said first dielectric layer;

(d.) applying and curing spin-on glass, to form a third dielectric layer to produce a dielectric stack including said third dielectric layer over said first and second dielectric layers, said third dielectric layer having a thickness equal to or greater than said second layer;

(e.) performing a global etchback to substantially remove said dielectric stack from high points of said partially fabricated structure, wherein at least a portion of said third dielectric layer remains after said global etchback;

(f.) deposition of an interlevel dielectric at least over said remaining second dielectric layer;

(g.) etching holes in said interlevel dielectric in predetermined locations; and

(h.) depositing and patterning a metallization layer to form a desired pattern of connections, including connections through said holes.

16. The integrated circuit of claim 15, wherein said deposition step (c.) is plasma-enhanced.

17. The integrated circuit of claim 15, wherein said deposition step (c.) uses TEOS as a source gas.

18. The integrated circuit of claim 15, comprising the additional step of applying a passivating dielectric, under vacuum conditions, after said step (a.) and before said deposition step (b.).

19. The integrated circuit of claim 15, wherein said deposition step (b.) applies said spin-on glass with a thickness in the range of 1000–5000 Å inclusive.

20. The integrated circuit of claim 15, wherein said interlevel dielectric is a doped silicate glass.

21. The integrated circuit of claim 15, wherein said deposition step (d.) applies said spin-on glass with a thickness in the range of 1000–5000 Å inclusive.

22. An integrated circuit, comprising:

(a.) an active device structure, including therein a substrate, active device structures, isolation structures, and one or more patterned thin film conductor layers including an uppermost conductor layer; and

(b.) a planarization structure, overlying recessed portions of said active device structure, comprising a layer of sol-gel-deposited dielectric overlain by a layer of vacuum-deposited dielectric overlain by a further layer of sol-gel-deposited dielectric;

(c.) an interlevel dielectric overlying said planarization structure and said active device structure, and having via holes therein which extend to selected locations of said uppermost conductor layer; and

(d.) an additional thin-film patterned conductor layer which overlies said interlevel dielectric and extends through said via holes to said selected locations of said uppermost conductor layer.

23. (Cancelled) A method, comprising:

forming a first layer of inorganic spin-on glass on a substrate;

depositing a first dielectric on the first layer;

forming a second layer of inorganic spin-on glass on the first dielectric; and

planarizing the second layer of spin-on glass.

24. (Cancelled) The method of claim 23 wherein forming the first layer of spin-on glass comprises depositing a siloxane-based spin-on glass on the substrate.

25. (Cancelled) The method of claim 23 wherein forming the first layer of spin-on glass comprises depositing a polyimide spin-on glass on the substrate.

26. (Cancelled) The method of claim 23 wherein forming the first layer of spin-on glass comprises depositing a polymethylmethacrylate spin-on glass on the substrate.

27. (Cancelled) The method of claim 23 wherein forming the first layer of spin-on glass comprises curing the first layer at 425°C.

28. (Cancelled) The method of claim 23, further comprising:

forming a second dielectric on the substrate before forming the first layer of spin-on glass; and

forming the first layer of spin-on glass on the second dielectric.

29. (Cancelled) The method of claim 23, further comprising:

forming a layer of metal on the substrate before forming the first layer of spin-on glass; and

forming the first layer of spin-on glass on the layer of metal.

30. (Cancelled) The method of claim 23, further comprising:

forming a layer of metal on the substrate before forming the first layer of spin-on glass;

depositing a second dielectric on the layer of metal before forming the first layer of spin-on glass; and

forming the first layer of spin-on glass on the second dielectric.

31. (Cancelled) The method of claim 23 wherein depositing the first dielectric comprises performing a plasma-enhanced deposition of the first dielectric onto the first layer of spin-on glass.

32. (Cancelled) The method of claim 23 wherein depositing the first dielectric comprises depositing an oxide onto the first layer of spin-on glass.

33. (Cancelled) The method of claim 23 wherein depositing the first dielectric comprises depositing a low-temperature oxide onto the first layer of spin-on glass.

34. (Cancelled) The method of claim 23, further comprising planarizing the first dielectric while planarizing the second layer of spin-on glass.

35. (Cancelled) The method of claim 23, further comprising planarizing the first dielectric and the first layer of spin-on glass while planarizing the second layer of spin-on glass.

36. (Cancelled) The method of claim 23 wherein planarizing the second layer of spin-on glass comprises etching back the second layer of spin-on glass.

37. (Cancelled) The method of claim 23, further comprising:

wherein planarizing the second layer of spin-on glass comprises etching back the second layer of spin-on glass; and

etching back the first dielectric while etching back the second layer of spin-on glass.

38. (Cancelled) The method of claim 23, further comprising:

wherein planarizing the second layer of spin-on glass comprises etching back the second layer of spin-on glass; and

etching back the first dielectric and the first layer of spin-on glass while etching back the second layer of spin-on glass.

39. A semiconductor structure, comprising:

a substrate;

a first layer of inorganic spin-on glass disposed on the substrate;

a first dielectric disposed on the first layer; and

a planarized second layer of inorganic spin-on glass disposed on the first dielectric.

40. The semiconductor structure of claim 39 wherein the first layer of spin-on glass comprises a siloxane-based spin-on glass.

41. The semiconductor structure of claim 39 wherein the first layer of spin-on glass comprises a polyimide spin-on glass.

42. The semiconductor structure of claim 39 wherein the first layer of spin-on glass comprises a polymethylmethacrylate spin-on glass.

43. The semiconductor structure of claim 39, further comprising:

a second dielectric disposed on the substrate; and

wherein the first layer of spin-on glass is disposed on the second dielectric.

44. The semiconductor structure of claim 39, further comprising:

a metal layer disposed on the substrate; and

wherein the first layer of spin-on glass is disposed on the metal layer.

45. The semiconductor structure of claim 39, further comprising:
a metal layer disposed on the substrate;
a second dielectric disposed on the metal layer; and
wherein the first layer of spin-on glass is disposed on the second dielectric.

46. The semiconductor structure of claim 39 wherein the first dielectric comprises a low-temperature oxide.

47. The semiconductor structure of claim 39, further comprising a planarized boundary that includes the planarized second layer of spin-on glass and a planarized portion of the first dielectric.

48. The semiconductor structure of claim 39, further comprising a planarized boundary that includes the planarized second layer of spin-on glass, a planarized portion of the first dielectric, and a planarized portion of the first layer of spin-on glass.